Datasheet

GW3323

RISC-V based 32-bit MCU with Bluetooth

Version: V0.2

1 Product Features

CPU and Flexible IO

- 32bit High performance CPU
- Program memory: internal 8M bit flash
- 256 Kbytes of SRAM
- Flexible GPIO pins with Programmable pull-up and pull-down resistors
- Support GPIO wakeup or interrupt
- 160 MHz maximum frequency

Bluetooth Radio

- Compliant to Bluetooth 5.2 and BLE specification
- TX output power MAX +9dBm
- RX Sensitivity with -94dBm @2M EDR

Supports

- A2DP /PBAP /HSP/ SPP

Peripheral and Interfaces

- Three 32-bit timers
- Three multi-function 32-bit timers, support Capture and PWM mode
- WatchDog
- Three full-duplex UART and one high speed serial port
- One SPI
- SD Card Host controller
- Full speed USB 2.0 HOST/DEVICE controller
- Sixteen Channels 10-bit ADC
- Two Channels 16-bit DAC
- Build in PMU, such as charger/buck/LDO

Package

- QFN40

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

Contents

2 Product information

See the following table for GW3323 product functions and peripheral configuration.

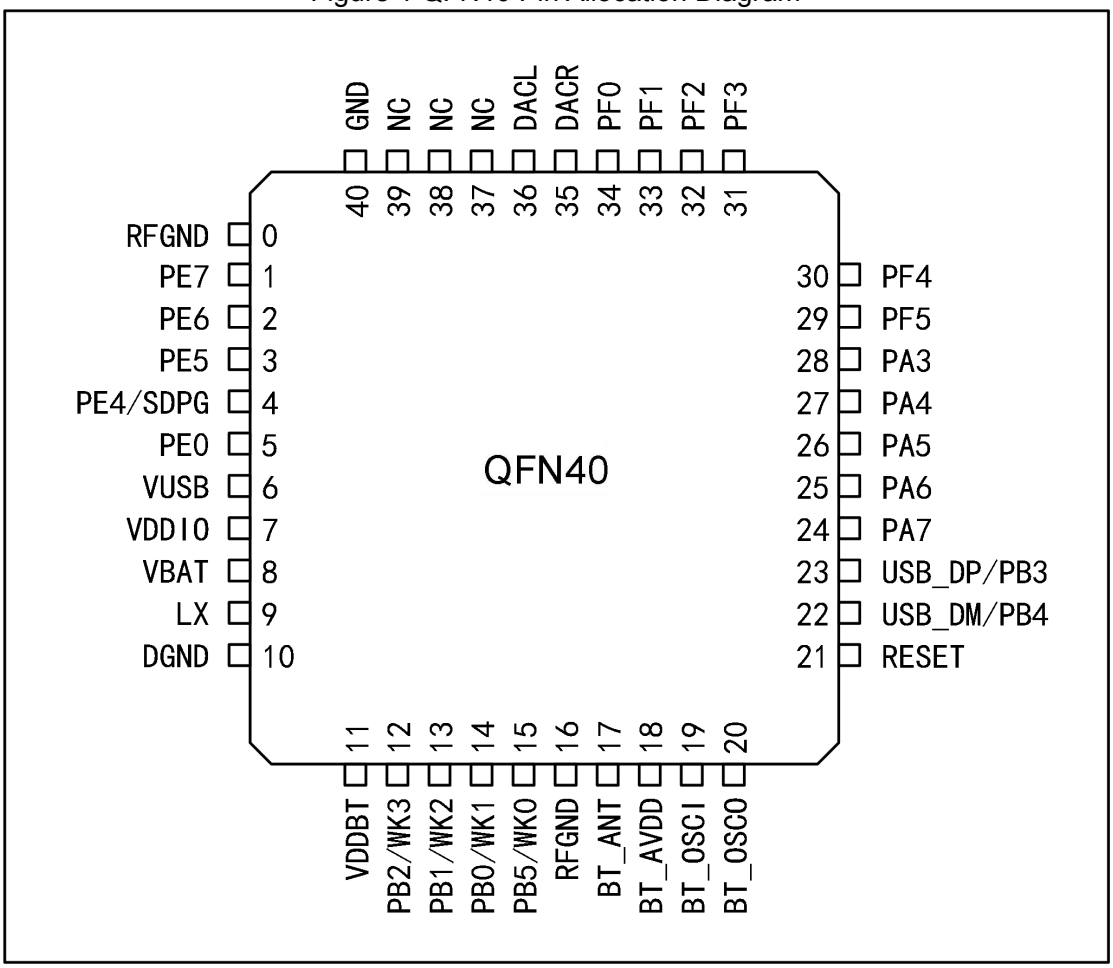
Table 1 Functions and Peripherals of GW3323 product

Model		**GW3323HGU6**
Package		QFN40
CPU@Max. frequency		RISCV@160MHz
Operating voltage		3.0V ~ 4.5V
Flash		1MB
SRAM		256KB
GPIOs		24
Communication interface	SPI	1
	I2C	1
	UART	3
	HSUART	1
	USB2.0 FS	1
	BT	1 BLE+1 SPP
Timer	32-bit general	3
	32-bit advanced	3
	Watchdog	1
	RTC	1
ADC	Channel	16
DAC	Channel	2

3 Pin information

3.1 Pin Figure

Figure 1 QFN40 Pin Allocation Diagram



3.2 Pin Descriptions

Table 2 QFN40 pin description

Pin No.	Name	Type	Function
0	RFGND	GND	BT RF Ground
1	PE7	I/O	SDDAT-G3 SPI1DO-G4 TX0-G4 HSTRX-G4 PWM2-T4-G1 IIC_DAT-G5 ADC-CH9 TMR4CAP_G1 PE7
2	PE6	I/O	SDCLK-G3 SPI1CLK-G4 RX0-G4 HSTRX-G9 PWM1-T4-G1 IIC_CLK-G5 IIC_CLK-G6 ADC-CH8 TMR3CAP_G7 PE6
3	PE5	I/O	SDCMD-G3 SPI1DI-G4 PWM0-T4-G1 IIC_DAT-G6 ADC-CH7 TMR3CAP_G6 PE5
4	PE4/SDPG	I/O	SDPG PWM1-T3-G4 PE4
5	PE0	I/O	SPI0DI-G3 TX0-G5 PWM0-T3-G4 TMR3CAP_G5 PE0

Pin No.	Name	Type	Function
6	VUSB	PWR	VUSB power input TX0-G8 TX1-G3 TX2-G3 HSTRX-G11 ADC-CH15
7	VDDIO	PWR	VDDIO power output,3.3V
8	VBAT	PWR	ADC-CH14 VBAT power input
9	LX	PWR	Buck inductor connect pin,power out.
10	DGND	GND	Digital Ground
11	VDDBT	PWR	BT power(1.2V)
12	PB2/WK3	I/O	SDDAT-G2 SPI1DO-G3 TX0-G2 TX2-G2 HSTRX-G2 PWM2-T3-G1 IIC_DAT-G3 ADC-CH4 WK3 PB2
13	PB1/WK2	I/O	SDCLK-G2 SPI1CLK-G3 RX0-G2 RX2-G2 HSTRX-G7 PWM1-T3-G1 IIC_CLK-G3 IIC_CLK-G4 ADC-CH3 TMR3CAP_G4 WK2 PB1
14	PB0/WK1	I/O	WK1 SPI1DI-G3

Pin No.	Name	Type	Function
			PWM0-T3-G1 IIC_DAT-G4 ADC-CH11 TMR3CAP_G3 PB0
15	PB5/WK0	I/O	PWM2-T3-G2 ADC-CH12 WKO PB5
16	RFGND	GND	BT RF Ground
17	BT_ANT	A	BT ANT
18	BT_AVDD	PWR	BT RF Power, power input,1.2V,connect with VDDBT
19	BT_OSCI	A	24M OSC input
20	BT_OSCO	A	24M OSC output
21	Reset	A	reset PIN(low level enable)
22	PB4/USB_DM	I/O	USB DM SDDAT-G4 SDDAT-G6 SPI0CLK-G3 RX0-G3 HSTRX-G8 PWM1-T3-G2 IIC_DAT-G8 ADC-CH6 PB4
23	PB3/USB_DP	I/O	USB DP SDDAT-G5 SDCMD-G6 SPI0DO-G3 TX0-G3 HSTRX-G3 PWM0-T3-G2 IIC_CLK-G8 ADC-CH5 PB3

Pin No.	Name	Type	Function
24	PA7	I/O	SDDAT-G1/G7 SPI1DO -G2 TX0-G1(RX) TX1-G1(RX) HSTRX-G1 PWM2-T5-G1 IIC_DAT-G1 ADC-CH2 PA7
25	PA6	I/O	SDCLK-G1/G4/G5/G6 SPI1CLK-G2 RX0-G1 RX1-G1 HSTRX-G6 PWM1-T5-G1 IIC_CLK-G1/G2 ADC-CH1 TMR3CAP_G2 PA6
26	PA5	I/O	SDCMD-G1/G4/G5 SPI1DI-G1 SPI1DI-G2 PWM0-T5-G1 IIC_DAT-G2 ADC-CH0 TMR3CAP_G1 PA5
27	PA4	I/O	SPI1DO -G1 TX1-G2 PWM2-T3-G3 PA4
28	PA3	I/O	SPI1CLK-G1 RX1-G2 PWM1-T3-G3 PA3
29	PF5	I/O	SDCMD-G7 SPI1DO -G5 TX0-G7

Pin No.	Name	Type	Function
			PWM1-T5-G2 IIC_DAT-G7 ADC-CH10 PF5
30	PF4	I/O	SDCLK-G7 SPI1CLK-G5 PWM0-T5-G2 IIC_CLK-G7 PF4
31	PF3	I/O	PWM2-T4-G2 PF3
32	PF2	I/O	PWM1-T4-G2 PF2
33	PF1	I/O	SPI1DI-G5 TX0-G6 PWM0-T4-G2 TMR5CAP_G1 PF1
34	PF0	I/O	PWM0-T3-G3 PF0
35	DACR	A	DAC0
36	DACL	A	DAC1
37	NC	-	-
38	NC	-	-
39	NC	-	-
40	GND	GND	Ground

Note:

(1) I/O: Digital input/output; I : Digital input; A : Analog Pin; PWR: Power Pin; GND: Ground.

(2) If you want to reuse GPIOx as SPI, IIC and other function pins, you need to add gpio_func_mapping() after the GPIO pin initialization function.

(3) G1~G9 are the numbers of peripheral mapping (gpio_func_mapping) to different IO.

(4) T0/1/2/3/4/5 represents the timer.

(5) CH0~CH15 represent the number of ADC channels.

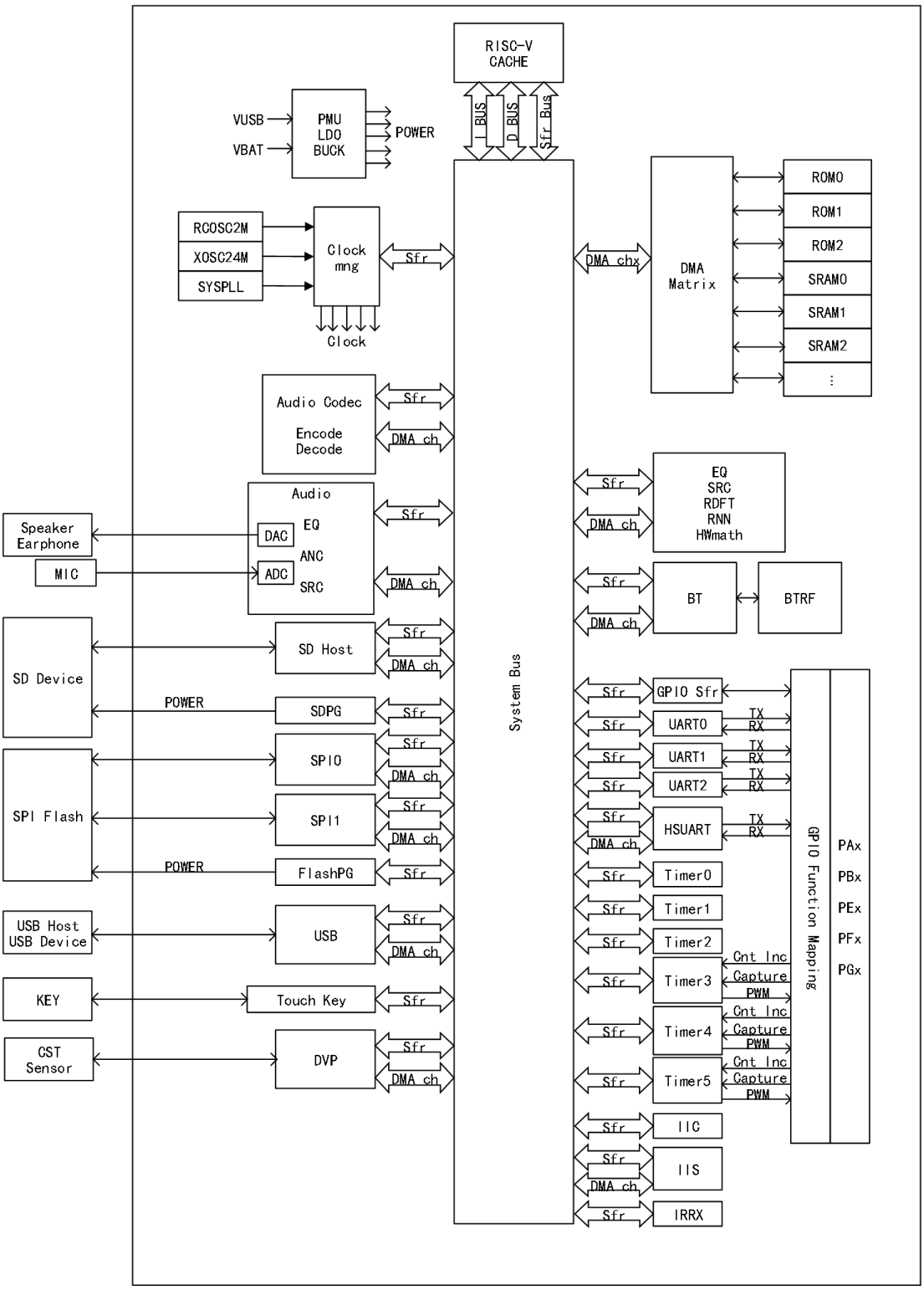
(6) TX0-G1 (RX) represents Channel 1 of serial port 0. This pin can be used as the receiving and transmitting pins for single-wire mode of the serial port (transmitting and receiving share the same wire).

4 Functional Description

4.1 System architecture

4.1.1 System Block Diagram

Figure 2 GW3323 System Block Diagram



Note: Chx indicates the channel number x

4.1.2 Address mapping

Table 3 GW3323HGU6 Memory Mapping

Start Address	Address	Name	Size	Include Register
0 (Register - 4KB)	0x00	SFR0	256B	TICK0\UART0-1\RTC\WDT\TMR0-2\SPI0
	0x100	SFR1	256B	DAC
	0x200	SFR2	256B	-
	0x300	SFR3	256B	USB\PLL\CLK\PWR\LVD\RST
	0x400	SFR4	256B	PIC
	0x500	SFR5	256B	ADC\WKUP
	0x600	SFR6	256B	GPIOA-F
	0x700	SFR7	256B	GPIOG
	0x800	SFR8	256B	IRRX\USERKEY\PROT
	0x900	SFR9	256B	TIM3-5\UART2\SPI1\RTC
	0xa00	SFR10	256B	TK\PIAN\TONEDLY\TKA
	0xb00	SFR11	256B	-
	0xc00	SFR12	256B	-
	0xd00	SFR13	256B	-
	0xe00	SFR14	256B	-
	0xf00	SFR15	256B	-
0x00001000		-		
0x00010600 (SRAM-190.5KB)	0X10600	cache	512B	cache_stack for loader
	0x10800	stack	1K	stack_ram，To avoid defining large parts in a function buf
	0x10c00	heap	12KB	heap
	0x13c00	data	13KB	Global variable, static variable, variable without AT.(uninitialized)
	0x17000	comm	36KB	Interrupt and various interrupt detection codes, storage com_text, com_rodata,variable without AT.(initialized)
	0x20000	bram	48KB	It was originally stored in "Bluetooth bottom layer, operating system and public area"; Users who do not use Bluetooth can assign at will.
	0x2c000	cram	80KB	Areas available to users,buff for storing ble.
0x00040000		-		
0x00050000 (SRAM-49.2KB)	0x50000	aram	16KB	Users can also use.
	0x54000	eram	0xa00=2.5KB	fot_data, the upgraded data must be retained.
	0x54a00	-	1KB	Reserve
	0x55000	rdftram	0x800=2KB	

Start Address	Address	Name	Size	Include Register
	0x55800	rram	608	for rnn input/output.(rnn algorithm) software cannot be accessed.
	0x58000	dram	0x4500=17.2KB	It is also available to users
	0x5c500	-		Reserve
0x00060000	0x60000	icram	32KB	
0x10000000 （flash-1MB）	0x10000000	init	512B	Store reset settings.
	0x10000200	flash(rx)	511.5KB	Functions without AT, text\rodata is stored here.
	0x10080000		492KB	The data in the backup area is generally placed from here.
	0x100fb000	cm	20KB	System parameter area (write data to cache, etc.) at least 20k.
0x10100000				

AT is a memory management mechanism that places corresponding codes or global variables in corresponding memory segments. The global variables without the AT will be placed in the common area of RAM. If the common area cannot hold them, they will be placed in FLASH, and it will be relatively slower to read variables from FLASH.

Figure 3

```
.comm : {
    *(.vector)
    *(.plt)
    *(.com_text*)
    *(.com_text.stack.handler)
    *(.com_rodata*)
    *debug.o(.rodata*)
    *(.data*)
    *(.sdata*)
    *(.load_text)
    *(.load_rodata)
    . = ALIGN(512);
} > comm AT > flash
```

Figure 4

```
.bram __bram_vma (NOLOAD) : {
    *(.btmem.bthw)
    *(.btmem*)

    *(.ble_cache*)
    *(.ble_buf*)
    *(.spp_tx_buff.*)
    *(.ble_tx_buff.*)
} > bram
```

4.2 Interrupt controller

4.2.1 Nested Vectored Interrupt Controller (NVIC)

GW3323 can handle up to 32 maskable interrupt channels and 1 priorities. The priority of peripheral access memory is 0. The interrupt vector entry address can be directly passed to the core, so that the interrupt response processing with low delay can give priority to the late higher-priority interrupt.

4.3 Power supply and power supply management

4.3.1 Power supply scheme

Table 4 Power Supply Scheme

Name	Voltage range	Description
Vbat	3.0V ~ 4.5V	After Vbat is powered, there are three LDO inside the chip for output to the IO port (3.3V, 150mA), Bluetooth module (1.2V), and core driver (1.1V) respectively
Vusb	4.6V~5.5V	Power supply for this pin is used to charge the lithium battery connected to the Vbat pin. If Vusb is powered and Vbat is not powered, this chip cannot start due to no power supply.

4.3.2 Charging management

This chip integrates a power management circuit internally, and it can charge 4.2V lithium batteries. The following modes and gears can be selected:

Constant charging current: 16 gears, 10~200mA.

Trickle charging current: 3 gears, 10~30mA.

Turn-off charging current: 8 gears, 2.5~35mA.

Turn-off charging voltage: 2 gears, 4.2V or 4.3V.

Trickle charging voltage: 2 gears, 2.9V or 3.0V.

4.4 Low-power mode

This chip supports two low-power modes. Users can switch between these modes by setting.

Table 5 Low-power Modes

Mode type	Description
Sleep mode	500uA, wake-up through Bluetooth, wake-up through external interrupt edge of ports (PA7, PB1, PB2, PB3, PB4, PB5, INT_FALL, INT_RISE), RTC or alarm wake-up.
Power-down mode	4uA, wake-up through external port interrupt edge of ports (VUSB, PB0, PB1, PB2, PB5), RTC, or alarm wake-up.

4.5 DMA

The product has 4-channel general-purpose DMA, which supports the data transmission from device to memory and from memory to device.

Each channel has hardware DMA request logic, and the source address, destination address and transmission length of each channel can be set separately by software.

DMA can be used for main peripherals of HSUART, SPI, SDIO, USB.

4.6 Communication peripherals

4.6.1 I2C bus

I2C bus is a two-wire serial interface, which consists of serial data line (SDA) and serial clock (SCL). No hardware CRC generator/calibrator.

4.6.2 Universal asynchronous receiver/transmitter (UART)

Embedded with 3 UART communication interfaces and 1 high-speed serial port HSUART. The HSUART interface can support DMA.

4.6.3 Serial peripheral interface (SPI)

Embedded with 1 SPI interface. Can be configured as master mode. The SPI1 receiving interface supports DMA operation, while the transmitting interface does not support DMA operation.

4.6.4 Universal Serial Bus (USBD)

The product is embedded with the module USBD compatible with full-speed USBD devices, which complies with the standard of full-speed USBD devices (12 Mbit/s), and the endpoints can be configured by software, and have standby/wake-up functions.

4.6.5 Bluetooth (BLE+SPP)

This chip has 1 built-in Bluetooth module that is compatible with Bluetooth 5.2 and BLE protocol specifications; maximum value of TX output power +9dBm; the receiving sensitivity is -94dBm at 2Mbit/s EDR. It can simultaneously support connection to 1 classic Bluetooth (SPP) and 1 low-power Bluetooth (BLE).

4.7 Analog peripherals

4.7.1 ADC (Analog/Digital Converter)

Integrate one 10-bit accuracy 16-channel ADC; each ADC can realize single-mode conversion.

4.7.2 DAC (Digital/Analog converter)

Integrate two 16-bit accuracy DAC.

4.8 Timer

The product includes 3 general-purpose timers (TMR0/1/2) and 3 advanced timers (TMR3/4/5).

Table 6 Function Comparison of Advanced and General-purpose Timers

Timer type	**General-purpose timer**			**Advanced timer**		
Timer name	TMR0 (system tick clock)	TMR1	TMR2	TMR3	TMR4	TMR5
Counter resolution	32 bits			32 bits		
Counter type	Up, down, up/down			Up, down, up/down		
Prescaler factor	N/A			N/A		
Clock Source	Incsrc (1MHz), Sysclk (up to 160MHz)			Incsrc (1MHz), Sysclk (up to 160MHz)		
Generate DMA request	No			No		
Capture/compare register	0			3*3		
Complementary output	None			None		
Pin characteristics	Each timer has 3-channel pins			Each timer has 3-channel pins		
Functional Description	No PWM			Can be used to generate PWM output\capture mode		

4.9 Watchdog (WDT)

A watchdog is built in this chip and can be used to detect and remove faults caused by software errors; when the counter reaches the given timeout value (2048ms by default), an interrupt will be triggered (only applicable to the window watchdog) or a system reset will be generated.

5 Characteristics

5.1 PMU Parameters

Table 7 PMU voltage input Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VUSB	Charger Voltage input	4.6	5.0	5.5	V	
VBAT	Voltage input	3.0	3.7	4.5	V	

Table 8 3.3V LDO Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VDDIO	3.3V LDO voltage output	-	3.3	-	V	Light Loading condition
△VVDDIO	Output Mismatch 1-sigma	-	43	-	mV	VDDIO=3.3v
ILOAD	Maximum output current	-	-	150	mA	@VBAT=3.6v
ISC	Short Circuit Current Limit	-	-	300	mA	@VBAT=3.8v

Table 9 1.2V LDO Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VDDBT	1.2V LDO voltage output	-	1.2	-	V	Light Loading condition
△VVDDBT	Output Mismatch 1-sigma	-	16	-	mV	VDDBT=1.2v
ILOAD	Maximum output current	-	-	100	mA	@VBAT=3.0v
ISC	Short Circuit Current Limit	-	-	200	mA	@VBAT=3.8v

Table 10 1.1V LDO Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
VDDCORE	1.1V LDO voltage output	-	1.1	-	V	Light Loading condition
△VVDDCORE	Output Mismatch 1-sigma	-	15	-	mV	VDDCORE=1.1v
ILOAD	Maximum output current	-	-	60	mA	@VBAT=3.6v
ISC	Short Circuit Current Limit	-	-	120	mA	@VBAT=3.8v

5.2 IO Parameters

Table 11 DAC Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
DAC	Maximum output current	-	-	50	mA	@VBAT=3.6v

Table 12 I/O Parameters

GPIO—Electrical Characteristics							
Symbol	**Description**	**Related GPIO**	**Min**	**Typical**	**Max**	**Units**	**Conditions**
VIL	Low-level input voltage		-0.3		1.27	V	VDDIO=3.3V
VIH	High-level input voltage		2.03		3.6	V	VDDIO=3.3V
Driver Ability 1	Output Driver Ability 1			32		mA	VDDIO=3.3V
Driver Ability 0	Output Driver Ability 0			8		mA	VDDIO=3.3V
RPUP0	Internal pull-up resister 0		8	10	12	KΩ	
RPUP1	Internal pull-up resister 1		0.24	0.3	0.36	KΩ	
RPUP2	Internal pull-up resister 2		160	200	240	KΩ	
RPDN0	Internal pull-down resister 0		8	10	12	KΩ	
RPDN1	Internal pull-down resister 1		0.24	0.3	0.36	KΩ	
RPDN2	Internal pull-down resister 2		160	200	240	KΩ	

5.3 BT Parameters

Table 13 BT Parameters

Characteristics	Min	Typical	Max	Unit	Conditions
Transmit Power	-	8	9	dBm	
RMS DEVM	-	5.5	-	%	Maximum TX power 2-DH5 packet
Peak DEVM	-	12.5		%	
EDR Relative Transmit Power		-0.2		dB	
Sensitivity @ Basic Rate		-91.8		dBm	BER=0.1%, using DH5 packet
Sensitivity @ EDR		-94		dBm	BER=0.01%, using 2-DH5 packet

5.4 Current Parameters

Table 14 Current Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
IRTC	RTC mode current	-	4	-	uA	4.2V input, room temp.
Sleep	Sleep current	-	500	2000	uA	3.3V input, room temp

6 Precautions for drawing board

6.1 Crystal oscillator

Since capacitors can be configured in the chip, the crystal oscillator selected can be within 9ppm; not needing to connect the capacitors at both ends of the crystal oscillator to the ground in parallel to prevent jittering.

Specification of crystal oscillator: 24M_9pF or 7.5pF load_+-10ppm.

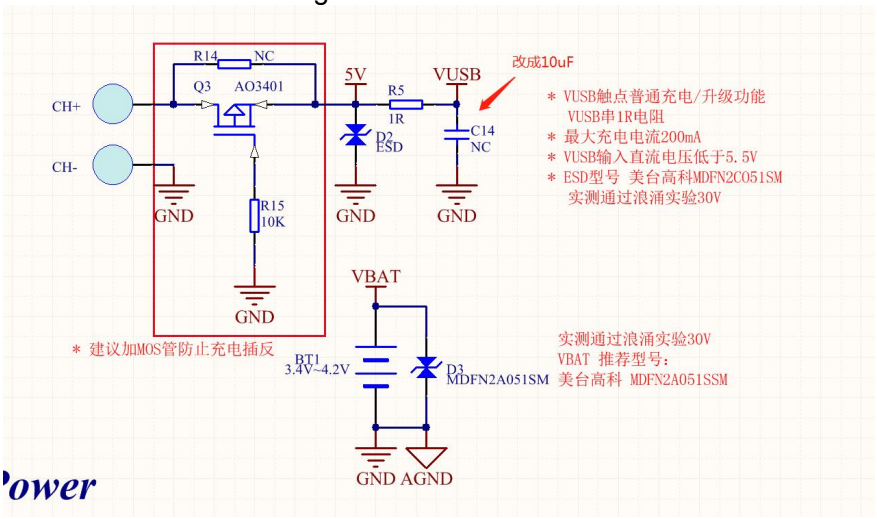
6.2 Capacitor

The decoupling capacitor of the master control (capacitor connected on VBAT/VDDIO/VDDBT/BT_AVDD/VDDDAC) shall be as close as possible to the main control and the circuit shall be as short as possible.

6.3 TVS protection

When USB is plugged, if the surge is too large, the chip will be burnt out, so it is recommended to add TVS protection when VUSB is directly connected to 5V. The specific circuit is as follows:

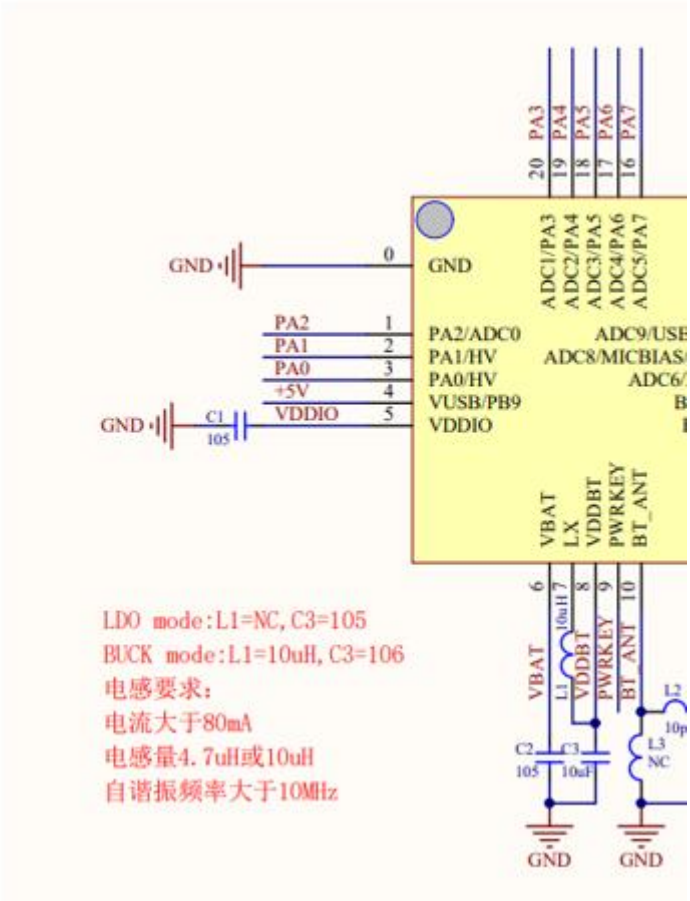
Figure 5 TVS Protection



D2 and D3 models are recommended to be “MDFN1610A051SA”\“MDFN1610A071SA”\“MDFN2C051SM2”

6.4 LX inductor

Figure 6 LX Inductor



Before the chip enters sleep mode, the Bluetooth will switch to buck mode and L1 on the hardware circuit must be connected; otherwise, "the Bluetooth module will be abnormal, or the Bluetooth performance may be reduced".

Requirements for L1 inductor: The power inductance is 10uH, the current is greater than 80mA, and the self-resonant frequency is greater than 10MHz;

Refer to models “MWPE0603D-100K-T” and “MWPE0805D-100K-T”.

The LX inductor is the inductor of the buck circuit inside the chip. If the buck circuit is not used, this inductor will be suspended.

6.5 Welding temperature

The welding temperature is recommended to be 260℃

7 Package Information

Figure 7 QFN40 Package Diagram

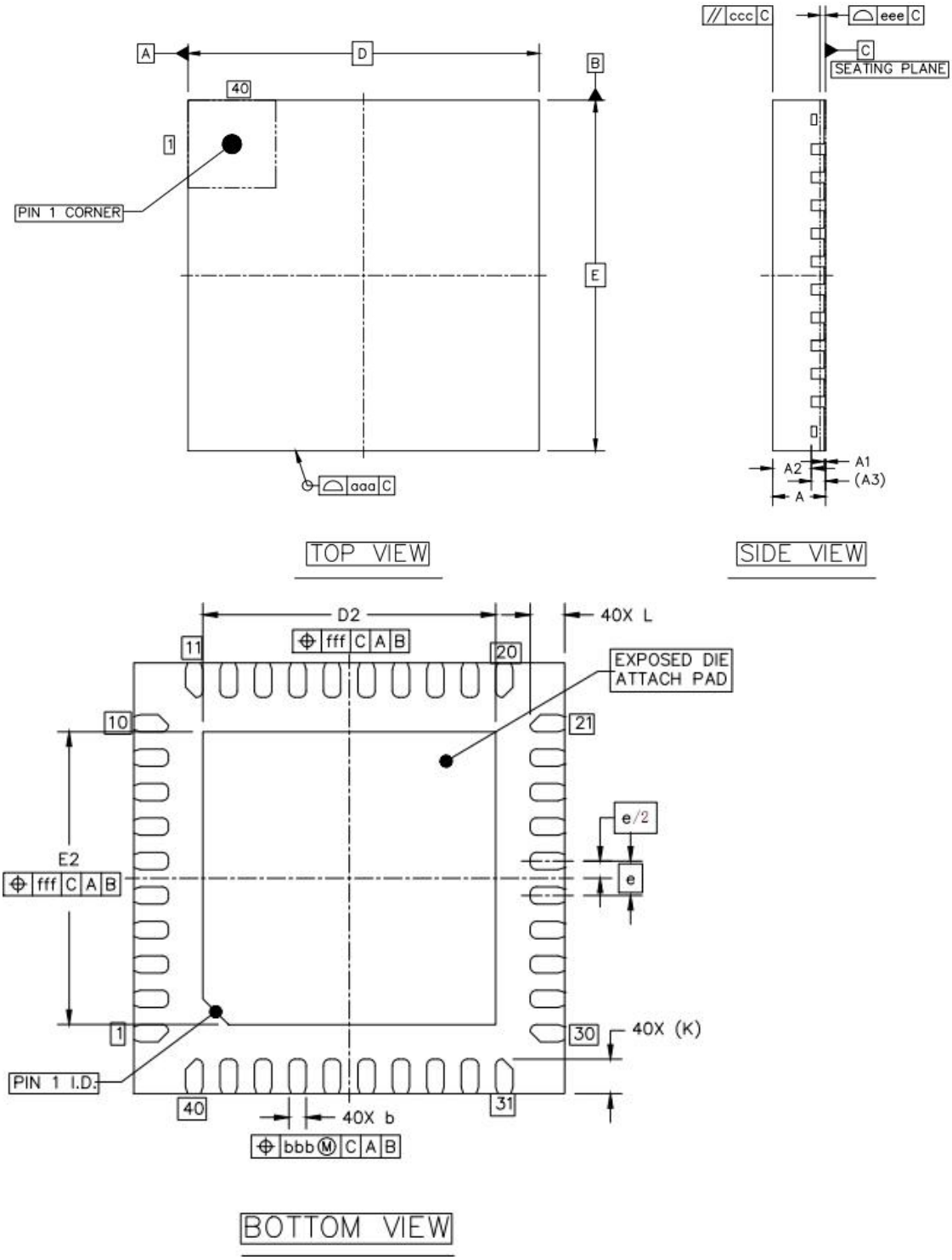


Table 15 QFN40 Packaging Data

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	3.3	3.4	3.5
	Y	E2	3.3	3.4	3.5
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.4 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

There is a gap in the antenna package, which is a problem of the drawing board, and this gap will not appear when the actual plate is hit, and will be automatically ignored..

8 Revision history

Table 16 Document Revision History

Date	Revision	Change History
2023.5.10	0.1	New
2023.9.13	0.2	Add introduction, function description, power management, artboard notes, ADC in pin definition, etc

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8. Scope of Application

The information in this document replaces the information provided in all previous versions of the document.